THAT WHICH IS CLAIMED IS:

1. A microprocessor comprising:

a processing unit;

a memory connected to said processing unit and comprising an addressable memory space for a lower memory area and an extended memory area;

means for connecting to and accessing said addressable memory space;

means for executing an instruction set for accessing said addressable memory space, the instruction set comprising a first instruction group for accessing said lower memory area, and a second instruction group distinct from the first instruction group for gathering instructions in the instruction set for accessing said extended memory area; and

means for preventing access to said extended memory area when executing the first instruction group.

2. A microprocessor according to Claim 1, wherein each location in said addressable memory space is associated with a respective access address; and further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing the first instruction group.

3. A microprocessor according to Claim 1, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

4. A microprocessor according to Claim 1, wherein each location in said addressable memory space is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area, the microprocessor further comprises means for maintaining an address of a jump destination location so that it points to a location in said lower memory area.

5. A microprocessor according to Claim 1, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area; and further comprising means for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area.

6. A microprocessor according to Claim 1, wherein the second instruction group comprises instructions for accessing said extended memory area in an indirect addressing mode.

7. A microprocessor according to Claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area.

8. A microprocessor according to Claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area.

9. A microprocessor according to Claim 1, wherein said means for connecting to and accessing said addressable memory space comprises an address bus; and further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space.

10. A microprocessor according to Claim 1, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

11. A microprocessor comprising:

a processing unit;

a memory connected to said processing unit and comprising an addressable memory space for a lower memory area and an extended memory area;

an address bus connected to said memory; and

an instruction set for accessing said addressable memory space, the instruction set comprising

a first instruction group for accessing said lower memory area,

a second instruction group distinct from the first instruction group for gathering instructions in the instruction set for accessing said extended memory area, and

instructions for preventing access to said extended memory area when executing the first instruction group.

12. A microprocessor according to Claim 11, wherein each location in said addressable memory space is associated with a respective access address; and wherein said instruction set further comprises instructions for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing the first instruction group.

13. A microprocessor according to Claim 11, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

14. A microprocessor according to Claim 11, wherein each location in said addressable memory space is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area, said

instruction set further comprises instructions for maintaining an address of a jump destination location so that it points to a location in said lower memory area.

15. A microprocessor according to Claim 11, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area; and wherein said instruction set further comprises instructions for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area.

16. A microprocessor according to Claim 11, wherein the second instruction group comprises instructions for accessing said extended memory area in an indirect addressing mode.

17. A microprocessor according to Claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area.

18. A microprocessor according to Claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area.

19. A microprocessor according to Claim 11, further comprising a program pointer register having a

size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space.

20. A microprocessor according to Claim 11, wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

21. A method for accessing a memory used by a microprocessor, the microprocessor comprising a processing unit, an address bus connected to the processing unit, with the memory being connected to the address bus and comprising an addressable memory space for a lower memory area and an extended memory area, the method comprising:

accessing the lower memory area using a first instruction group;

gathering instructions in the instruction set for accessing the extended memory area; and

preventing access to the extended memory area when executing the first instruction group.

22. A method according to Claim 21, wherein each location in the addressable memory space is associated with a respective access address; and further comprising instructions for forcing an access address of a location to be accessed to point to a location in the lower memory area when executing the first instruction group.

23. A method according to Claim 21, further comprising at least one internal register; and wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in the addressable memory space; and

data transfer instructions between the arbitrary memory location and the at least one internal register.

24. A method according to Claim 21, wherein each location in the addressable memory space is associated with a respective access address; and for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in the lower memory area, further comprising maintaining an address of a jump destination location so that it points to a location in the lower memory area.

25. A method according to Claim 21, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in the lower memory area; and further comprising forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in the lower memory area and points to this area.

26. A method according to Claim 21, wherein the second instruction group comprises instructions for accessing the extended memory area in an indirect addressing mode.

27. A method according to Claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located in the lower memory area.

28. A method according to Claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located within the extended memory area.

29. A method according to Claim 21, wherein the microprocessor further comprises a program pointer register having a size corresponding to a size of the address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in the addressable memory space.

30. A method according to Claim 21, wherein the lower memory area is accessible over 16 bits and the extended memory area is accessible over 24 bits.